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CLAIMS

1. A voltage reading enhancement system for an open digit line array DRAM device comprising a plurality of sub-arrays, the voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to decouple the component in the active sub-array from the corresponding component in the reference sub-array when the active row signal is received.

2. The voltage reading enhancement system of claim 1 wherein the component of the active sub-array comprises a cell plate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a cell plate of the reference sub-array.

3. The voltage reading enhancement system of claim 1 wherein the component of the active sub-array comprises a substrate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a substrate of the reference sub-array.

4. The voltage reading enhancement system of claim 1 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

5. The voltage reading enhancement system of claim 1 wherein the controller is responsive to direct the selective coupling device to recouple the component in the active sub-

array to the corresponding component in the reference sub-array when the active row signal is not received.

6. A voltage reading enhancement system for an open digit line array DRAM device comprising a plurality of sub-arrays, the voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a cell plate of an active sub-array to a corresponding cell plate of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to decouple the cell plate in the active sub-array from the corresponding cell plate in the reference sub-array when the active row signal is received.

7. The voltage reading enhancement system of claim 6 further comprising a second selective coupling device selectively electrically coupling a substrate of the active sub-array to a corresponding substrate of the reference sub-array.

8. The voltage reading enhancement system of claim 6 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

9. The voltage reading enhancement system of claim 7 wherein the second selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

10. The voltage reading enhancement system of claim 6 wherein the controller is responsive to direct the selective coupling device to recouple the cell plate in the active sub-

array to the corresponding cell plate in the reference sub-array when the active row signal is not received.

11. The voltage reading enhancement system of claim 7 wherein the controller is responsive to direct the second selective coupling device to recouple the substrate in the active sub-array to the corresponding substrate in the reference sub-array when the active row signal is not received.

12. A voltage reading enhancement system for an open digit line array DRAM device comprising a plurality of sub-arrays, the voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a substrate of an active sub-array to a corresponding substrate of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to decouple the substrate in the active sub-array from the corresponding substrate in the reference sub-array when the active row signal is received.

13. The voltage reading enhancement system of claim 12 further comprising a second selective coupling device selectively electrically coupling a cell plate of the active sub-array to a corresponding cell plate of the reference sub-array.

14. The voltage reading enhancement system of claim 12 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

15. The voltage reading enhancement system of claim 13 wherein the second selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

16. The voltage reading enhancement system of claim 12 wherein the controller is responsive to direct the selective coupling device to recouple the substrate in the active sub-array to the corresponding substrate in the reference sub-array when the active row signal is not received.

17. The voltage reading enhancement system of claim 13 wherein the controller is responsive to direct the second selective coupling device to recouple the cell plate in the active sub-array to the corresponding cell plate in the reference sub-array when the active row signal is not received.

18. An open digit line array DRAM device comprising:

a plurality of sub-arrays of memory cells, the memory cells being disposed in rows and columns;

a plurality of sense amplifiers disposed between the sub-arrays, each of the sense amplifiers receiving a first digit line from a column of memory cells in a first sub-array and second digit line from a column of memory cells in a second sub-array;

a row addressing system operably connected to the DRAM device, the row addressing system responsive to a row address signal by accessing a row in the DRAM device corresponding to the row address signal;

a refresh indicator signaling when a row of memory cells is to be refreshed;

a row refreshing circuit, operably connected with the row addressing system, the DRAM cells, and the refresh indicator, the row refreshing circuit directing a refresh of at least one row of memory cells in response to the refresh indicator signaling a row of memory cells is to be refreshed; and

a voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to decouple the component in the active sub-array from the corresponding component in the reference sub-array when the active row signal is received.

19. The open digit line array DRAM device of claim 18 wherein the component of the active sub-array comprises a cell plate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a cell plate of the reference sub-array.

20. The open digit line array DRAM device of claim 18 wherein the component of the active sub-array comprises a substrate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a substrate of the reference sub-array.

21. The open digit line array DRAM device of claim 18 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

22. The open digit line array DRAM device of claim 18 wherein the controller is responsive to direct the selective coupling device to recouple the component in the active sub-array to the corresponding component in the reference sub-array when the active row signal is not received.

23. A memory system comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of open digit line array DRAM device, each open digit line DRAM device comprising:

a plurality of sub-arrays of memory cells, the memory cells being disposed in rows and columns;

a plurality of sense amplifiers disposed between the sub-arrays, each of the sense amplifiers receiving a first digit line from a column of memory cells in a first sub-array and second digit line from a column of memory cells in a second sub-array;

a row addressing system operably connected to the DRAM device, the row addressing system responsive to a row address signal by accessing a row in the DRAM device corresponding to the row address signal;

a refresh indicator signaling when a row of memory cells is to be refreshed;

a row refreshing circuit, operably connected with the row addressing system, the DRAM cells, and the refresh indicator, the row refreshing circuit directing a refresh of at least one row of memory cells in response to the refresh indicator signaling a row of memory cells is to be refreshed; and

a voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the selective coupling device to

decouple the component in the active sub-array from the corresponding component in the reference sub-array when the active row signal is received.

24. The memory system of claim 23 wherein the component of the active sub-array comprises a cell plate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a cell plate of the reference sub-array.

25. The memory system of claim 23 wherein the component of the active sub-array comprises a substrate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a substrate of the reference sub-array.

26. The memory system of claim 23 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

27. The memory system of claim 23 wherein the controller is responsive to direct the selective coupling device to recouple the component in the active sub-array to the corresponding component in the reference sub-array when the active row signal is not received.

28. A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a system memory operably connected to the processor through a system bus, the system memory comprising a plurality of open digit line array DRAM devices having a plurality of rows of DRAM cells, the DRAM cells receiving, storing, and outputting data, the system memory comprising:

a memory controller;

a memory bus operably coupled with the memory controller to communicate memory commands from the memory controller and communicate memory output signals to the memory controller; and

a plurality of open digit line array DRAM device, each open digit line DRAM device comprising:

a plurality of sub-arrays of memory cells, the memory cells being disposed in rows and columns;

a plurality of sense amplifiers disposed between the sub-arrays, each of the sense amplifiers receiving a first digit line from a column of memory cells in a first sub-array and second digit line from a column of memory cells in a second sub-array;

a row addressing system operably connected to the DRAM device, the row addressing system responsive to a row address signal by accessing a row in the DRAM device corresponding to the row address signal;

a refresh indicator signaling when a row of memory cells is to be refreshed;

a row refreshing circuit, operably connected with the row addressing system, the DRAM cells, and the refresh indicator, the row refreshing circuit directing a refresh of at least one row of memory cells in response to the refresh indicator signaling a row of memory cells is to be refreshed; and

a voltage reading enhancement system comprising:

a selective coupling device selectively electrically coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

a controller coupled with the selective coupling device and operable to receive an active row signal, the active row signal indicating an active row of memory cells within the active sub-array is to be coupled with an active digit line, the controller being responsive to the active row signal to direct the

selective coupling device to decouple the component in the active sub-array from the corresponding component in the reference sub-array when the active row signal is received.

29. The computer system of claim 28 wherein the component of the active sub-array comprises a cell plate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a cell plate of the reference sub-array.

30. The computer system of claim 28 wherein the component of the active sub-array comprises a substrate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a substrate of the reference sub-array.

31. The computer system of claim 28 wherein the selective coupling device is a transistor the controller selectively causes to conduct when memory cells are not being read and selectively not to conduct when the memory cells are being read.

32. The computer system of claim 28 wherein the controller is responsive to direct the selective coupling device to recouple the component in the active sub-array to the corresponding component in the reference sub-array when the active row signal is not received.

33. A method for enhancing the accuracy of reading stored memory cell voltages in an open digit line array DRAM device, the method comprising:

coupling a component of an active sub-array to a corresponding component of a reference sub-array; and

selectively decoupling the component of the active sub-array from the corresponding component of the reference sub-array when an active row of memory cells within the active sub-array is to be connected to an active digit line.

34. The method of claim 33 wherein the component of the active sub-array comprises a cell plate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a cell plate of the reference sub-array.

35. The method of claim 33 wherein the component of the active sub-array comprises a substrate of the active sub-array, and wherein the corresponding component of the reference sub-array comprises a substrate of the reference sub-array.

36. The method of claim 33 wherein the component of the active sub-array is recoupled to the corresponding component of the reference sub-array when an active row of memory cells within the active sub-array is not to be connected to an active digit line.

37. A method for enhancing the accuracy of reading stored memory cell voltages in an open digit line array DRAM device, the method comprising:

coupling a cell plate of an active sub-array to a corresponding cell plate of a reference sub-array; and

selectively decoupling the cell-plate of the active sub-array from the corresponding cell plate of the reference sub-array when an active row of memory cells within the active sub-array is to be connected to an active digit line.

38. The method of claim 37 further comprising coupling a substrate of the active sub-array to a corresponding substrate of the reference sub-array.

39. The method of claim 37 wherein the cell plate of the active sub-array is recoupled to the corresponding cell plate of the reference sub-array when an active row of memory cells within the active sub-array is not to be connected to an active digit line.

40. The method of claim 38 wherein the substrate of the active sub-array is recoupled to the corresponding substrate of the reference sub-array when an active row of memory cells within the active sub-array is not to be connected to an active digit line.

41. A method for enhancing the accuracy of reading stored memory cell voltages in an open digit line array DRAM device, the method comprising:

coupling a substrate of an active sub-array to a corresponding substrate of a reference sub-array; and

selectively decoupling the substrate of the active sub-array from the corresponding substrate of the reference sub-array when an active row of memory cells within the active sub-array is to be connected to an active digit line.

42. The method of claim 41 further comprising coupling a cell plate of the active sub-array to a corresponding substrate of the reference sub-array.

43. The method of claim 41 wherein the substrate of the active sub-array is recoupled to the corresponding substrate of the reference sub-array when an active row of memory cells within the active sub-array is not to be connected to an active digit line.

44. The method of claim 42 wherein the cell plate of the active sub-array is recoupled to the corresponding cell plate of the reference sub-array when an active row of memory cells within the active sub-array is not to be connected to an active digit line.